REMARKS

Claims **1-20** are currently pending in the application. Claims **1** and **8** are amended to render the meaning of the claims clear and definite. The amendments which are for clarification purposes only are fully supported by at least page 5 of the specification, no new matter is added, and no issues are raised that would require further search. Reconsideration of the rejected claims in view of the above amendments and following remarks is respectfully requested.

Response to Advisory Action and Telephonic Interview with Examiner

In response to the Advisory Action and telephonic interview with the Examiner, Applicants submit that claim 13 was not amended and did not change its dependency from claim 10. This is evidenced by the word "original" prior to the recitation of claim 13. Applicants did note a typographical error, which is now corrected. Applicants submit that there is no new issues that need further search and/or consideration and that the amendment should now be considered and entered into the record.

35 U.S.C. § 1.112, Second Paragraph Rejection

Claims 1 and 8 were rejected under 35 U.S.C. § 1.112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In response, the limitation "said refresh rate" in lines 12-14 of claim 1 has been amended to read "a refresh rate" in order to provide proper antecedent basis. Claim 8 has been amended to recite:

> wherein said ECC memory allocation circuit reassigns said non-critical bit addresses as a second memory space designated for storing ECC parity bits.

Applicant respectfully submits that claim 8, as amended, is comprehensible. Accordingly, withdrawal of the § 1.112, second paragraph, rejections of claims 1 and 8 is respectfully requested.

35 U.S.C. § 102/103 Rejections

Claims 1-5, 7-11, 13, and 14 were rejected under 35 U.S.C. §102(e) for being unpatentable over U.S. Patent No. 6,697,992 B2 to Ito *et al.*("Ito"). Claims 6, 12, and 15-20 were rejected under 35 U.S.C. §103(a) over Ito. This rejection remains traversed.

Applicants submit that the rejections of claims 1-14 are rendered moot in view of the Declaration by the named inventor under 37 C.F.R. §1.131, which submitted with Applicants' response of September 9, 2004. More specifically, Applicants submit that the Rule 131 Declaration previously filed is formally and substantively sufficient to establish that the Inventor had conceived and reduced to practice with due diligence the invention defined in at least independent claims 1, 10, and 15 starting before the effective date of the primary reference to Ito, *i.e.*, August 8, 2001.

The Examiner asserts that Exhibit A lacks at least one element of claim 1 for reduction to practice, namely:

> a refresh execution circuit for reducing said refresh rate in said sleep mode and increasing said refresh rate in said active mode.

This assertion is respectfully traversed.

A person of skill in the DRAM art at the time the invention was made would understand Exhibit A as disclosing a refresh execution circuit for reducing the refresh rate during sleep mode, and increasing the refresh rate in active mode. Referring to Exhibit A, one of the features of developing low power DRAMS is a longer cell retention time to facilitate a slower refresh frequency in the end product application. This reduced the power associated with refreshing the DRAM. More specifically, Exhibit A, under Projected Benefit, clearly discloses that the refresh rate is reduced in sleep mode and increased in active mode. That is, there is a longer sleep mode (SM) retention time as shown in the example of 80 ms at 85°C and 600 ms at 40°C. This clearly shows a reduced refresh rate in the sleep mode.

A person of ordinary skill in the DRAM art would also understand, given Exhibit A, that the refresh rate is increased in active mode. Specifically, exhibit discloses that:

> Upon exiting SM, ECC is used to correct any retention time fails that occurred during sleep; ECC bits are discarded and the total DRAM becomes available for end application utilization (emphasis added).

This clearly implies that the refresh rate increases upon exiting sleep (SM). Normal operation of a DRAM requires that the DRAM be refreshed at a rate that satisfies the worst case retention time (80 ms as indicated on page 2 of the Office Action) for the cells in the DRAM over the whole operating temperature for the junction temperature of the device.

Thus, Exhibit A demonstrates that the inventor, at the time of the invention, from conception to reduction to practice, recognized the elements set forth in claims 1, 10, and 15. Accordingly, the previously filed 1.131 Affidavit and accompanying documents is sufficient to overcome the §102(e) rejection.

CONCLUSIONS

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submit that all of the stated assertions have been overcome or rendered moot. Applicants believe all of the claims to be allowable and in condition for allowance, the Examiner is respectfully requested to pass the above application to issue, and is invited to contact the undersigned at the telephone number listed below, if needed. Prompt and favorable consideration of this reply is respectfully requested. Please charge any deficiencies in fees and credit any overpayment of fees to **IBM Deposit Account No. 09-0458** (Fishkill).

Respectfully submitted,

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